Computer Science & Electrical Engineering Seminar Series

Digital Arithmetic: Architectures, Challenges and Implementations

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Digital arithmetic has continued to play an important role in the design of digital systems, microprocessors, microcontrollers, application specific integrated circuits (ASIC), and embedded systems which have applications in signal processing, graphics, and communications. In spite of a mature body of knowledge, each new generation of chips, microprocessors/microcontrollers or digital systems presents new arithmetic design challenges that need to be resolved. A good solution is often found in the best trade-off between speed, cost, power, and VLSI chip area.

Designing an efficient adder has been a major research topic since the digital integrated circuit was first developed. In the worst-case scenario of the conventional carry ripple binary adder, carry may propagate from the least significant to the most significant bit position through a bank of full adders causing a delay proportional to the adder size. Approaches such as the Carry Look-Ahead and the Parallel Prefix Tree adders are designed to reduce the latency at the expense of additional hardware overhead that complicates adder design and implementation. On the other hand, the Binary Signed Digit Number (BSDN) System, which is a non-conventional numbering system, can be used in adder design to restrict or eliminate the carry propagation chain by avoiding the dependency of the output on input carry signal. In order to use this numbering system, BSDN digits need to be encoded into binary bits. The selection process of the encoding scheme is very crucial since it affects the overall adder performance.

In this talk we will discuss the current digital arithmetic challenges and merits/demerits of existing adder architectures. New designs based on BSDN with two and three bit encodings will be presented. We will also present a Limited Selective Redundancy Injection (LSRI) method to introduce redundancy into conventional adder architectures with minimal hardware changes.

Prof. Ghulam Chaudhry

Prof. Ghulam M. Chaudhry received his M.Sc. degree in Electronics from Bahauddin Zakariya University, Multan, Pakistan in 1978, and M.S. and PhD degrees in Computer Engineering, from Wayne State University, Detroit, in 1986 and 1989. Currently, he is a full professor and the Associate Chair of the CSEE department in the School of Computing and Engineering, University of Missouri-Kansas City. His research interests include Computer Architecture and Parallel Processing, Performance of Multiprocessor Systems, Digital System Design, VLSI Design and Verilog HDL. He has published over a hundred research papers in peer-reviewed journals and national/international conferences. During his professional career he has received numerous awards including the Thomas Rumble Doctoral Fellowship Award 1988 at Wayne State University, Faculty Research Award 1997 and Good Teaching Award 2000 both at the University of Missouri-Columbia. Dr. Chaudhry has chaired many sessions in the conferences/symposia, in addition to acting as an overall chair for several conferences. Recently, he chaired the "2008 IEEE Region 5 BASICS^2" conference which was hosted by CSEE Department, UMKC, IEEE KC-Section, and IEEE Region 5. Dr. Chaudhry is a Senior Member of IEEE.

Fekri Kharbash

Fekri Kharbash received his B.S. degree in Electrical Engineering from United Arab Emirate University in 1999 and his M.Sc. degree also in Electrical Engineering from UMKC in 2004. Currently he is a PhD student in the School of Computing and Engineering (SCE) at UMKC. His research interests include digital arithmetic, computer architecture, and digital design. He has been a student member of the Institute of Electronic and Electrical Engineers (IEEE) since 2003.